CHAPTER MEETINGS

SCV-ComSoc - 5/30 | **Seminar: Mobile Broadband Ecosystem for the Pacific Rim** - 3G, 4G, WiMAX, LTE, lessons ... [more]

SCV-Phot - 6/2 | **Where in the Nano-world is Lithography Taking Us?** - fundamental physical limits, economic, technical issues ... [more]

SCV-MBS_CAS - 6/4 | **ELECTRIC: a Multithreaded Integrated-Circuit Design System** - open-source, Java, thin-client support ... [more]

SCV-TMC - 6/4 | **Goldilocks and the Three Bears: Optimal Development Processes for Startups, Large Companies** ... [more]

SCV-Section - 6/4 | **IEEE Senior Member Grade Elevation Night** - get upgraded! ... [more]

SF=PES - 6/7-11 | **IEEE Stationary Battery Technical Committee Meetings** - lead-acid, nuclear, NiCad, portable, UPS ... [more]

SCV-EDS - 6/9 | **Negative Bias Temperature Instability in p-MOSFETs** - characterization, materials dependence, modeling ... [more]

SF-ComSoc - 6/9 | **Internet 2.0: Hype or Hope?** - limitations, security, routing table size, address allocation ... [more]

SCV-CNSV - 6/9 | **The Life of SPICE** - journey of SPICE from teaching program to support and expansion ... [more]

SCV-ComSoc+CAS - 6/10 | **VoIP for Wireless** - transparent hand-offs, concurrent calls, measurements ... [more]

SCV-CPMT - 6/10 | **Wafer-Level Packaging – Next Turn in the Road** - DRAM, TSVs, burn-in, test, handling, alternative paradigms ... [more]

SPECTRUM - 6/11 | **Webcast: Multiphysics Simulation** - design problems, solutions, MEMS, heat transfer ... [more]

SCV-RAS - 6/11 | **Modular Robotics Technologies: Sculpting Behavior** - forming, testing, hands-on invention, learning ... [more]

OEB-IAS - 6/11 | **Motor Design Considerations for Above NEMA AC Induction Motors** - electrical design techniques, testing ... [more]

SCV-CNSV - 6/12 | **Communication Tools for Consultants** - working in a positive, productive, amicable way ... [more]

SCV-CNSV - 6/13 | **Marketing Your Consulting Services On Craig's List** - getting more successful; hands-on training ... [more]

SCV-CAS - 6/15 | **Renewable Energy** - oil demand, climate change, new jobs, opportunities ... [more]

SCV-Nano - 6/16 | **Nano-Solar Cells: Solar Cells of the Future with Nanotechnology** - dye-sensitized, quantum dot, hybrid ... [more]

SCV-SSC - 6/18 | **A Low-Power 60GHz Transceiver with Integrated Baseband Circuitry** - very low power, low BER ... [more]

SCV-SPS - 6/22 | **Adaptive Learning in a World of Projections** - set of solutions, training points, constraints, algorithms ... [more]

SF-PES - 6/24 | **Increasing Renewable Generation in California** - a key to meeting California and US carbon reduction targets ... [more]

SCV-CPMT - 6/25 | **License to Speed: Extreme-Bandwidth Packaging + Tour** - digital and analog, 80 GHz, low insertion loss ... [more]

SCV-CPMT - 9/9 | **Molecular Modification of PCB Substrates for Fine Line Patterning** - lithographic process, fine line spacing ... [more]

Conference Calendar

June 8-9: **4th Frontiers in Biomedical Devices Conference & Expo** - Hyatt Regency, Irvine [more]

June 24: **Multi-Network Operation: WiFi, WiMAX, 3G** - Hilton Garden Inn, San Mateo [more]

July 9-10: **IEEE Mobile WIMAX Symposium** - Meritage Hotel, Napa Valley [more]

July 19-23: **InterPACK: Packaging and Integration of Electronic and Photonic Systems, MEMS, and NEMS** - Westin St Francis, SF [more]

July 26-31: **46th IEEE Design Automation Conf (DAC)** - Moscone Convention Center, SF [more]

August 11-13: **4th Annual Flash Memory Summit** - Santa Clara Convention Center [more]

Sept 23-25: **CMOS Emerging Technologies Workshop** - Vancouver, BC, Canada [more]

Technical Training Course

Power Transformer, Fluid Diagnostics Seminars
-- June 8-11 -- San Francisco [more]

Tech Academy of Silicon Valley

Jr, Sr High Summer Academy Sessions [more]
-- 6th thru 11th grade students

Chapter Short Courses/Seminars

July 18: **The Future for Hand-Held Devices** [more]
- full-day seminar - at Stanford University

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From the Editor …

As I write this note, I'm sitting in a hotel, looking out over San Diego bay, while attending an IEEE conference. The miracles of modern technology – something to which most of you have been contributors.

There's a lot of focus were on mobile technology – handsets, lower power dissipation, denser packaging, more functionality, higher-energy power sources, better modeling/CAD tools, etc. We're trying to bring groupings of research results and topical papers into Special Sections in various of IEEE's Transactions. Your journals are a good place to look for new results that'll affect your own work.

Did you know that you can subscribe to a "feed" for each IEEE journal in which you have an interest? This can be a big help – every time a new issue is posted to IEEE's Xplore system, you get an email with a link to the Table of Contents. You can quickly jump to the website, scan the titles, read key abstracts, and download the papers of interest. It's the best way to see what your colleagues are doing in their labs and companies. To select journals to monitor, visit:

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Paul

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Sponsored by the Santa Clara Valley Section of IEEE

IEEE Senior Member Grade Elevation Night

Date: Thursday, June 4, 2009

Time: 6:15 – 8:00 PM (drop in at any time between 6:15 PM and 7:30 PM)

Location: Cogswell Polytechnical College, Executive Board Room

1175 Bordeaux Drive, Sunnyvale, CA 94089

Refreshments will be provided

The IEEE Santa Clara Valley Section, in conjunction with PACE, is sponsoring a **Senior Member Grade Elevation night** for all IEEE members who meet the requirements for grade elevation to Senior Member. The requirements are posted at

www.ieee.org/web/membership/senior-members

Summary:

* be an engineer, scientist, educator, or technical executive in IEEE-designated fields;
* have been **in professional practice** for:
  - **7 years** if you hold a baccalaureate degree in an IEEE-designated field;
  - **6 years** if you hold a baccalaureate and a masters degree;
  - **5 years** if you hold a doctorate
* show professional maturity and "significant performance" over a period of at least five of those years in professional practice.

IEEE members who meet these requirements are **encouraged to attend.** Potential Senior Members will have an opportunity to **meet with Senior Members** and possibly obtain Senior Member/Fellow references that are required for the application. If possible, please have another senior member or Fellow fill out a nomination form, on-line, prior to the event at:

http://www.ieee.org/web/membership/senior-members/application.html#nomination

This nomination helps in expediting the process. **Members must bring** 4 hard copies of the completed Senior Member Application Form found at:

www.ieee.org/web/membership/senior-members/application.html

(Print out, fill in the information, and bring 4 copies)

Also members are asked to **write a few sentences** on Page 2 of the Application, or else in a file on the flash memory device, explaining how they have significantly performed their professional duties for at least five years. However, please remember that the process is exploratory and references are not guaranteed. For any questions please send email to John Berg **ieeenano@gmail.com**

Become a Senior Member -- See you there!

Technical Training Course – June 8-11, 2009

POWER TRANSFORMERS SEMINAR
June 8-10, 2009

The Power Transformers Seminar will focus on maintaining and assessing the integrity of the critical component that dictates the life of a power transformer - the insulation system. Included will be a guided visit through Delta Star Inc., a manufacturer of power transformers and mobile substations in nearby San Carlos.
Participation in the factory tour is at the sole discretion of Delta Star

Topics covered:

- Transformer Design
- Insulation System Design
- Transformer Specification – What should be included to maximize the lifetime of your power transformer.
- Factory Inspection and Test
- Transformer Loading
- Transformer Maintenance
- Condition Assessment
- Moisture in Transformers
- Field Processing of Power Transformers
- High Temperature Insulation Systems
- Alternative Fluids
- Mobile substation design and manufacture

This 4-day technical course is designed for engineering, operations and maintenance personnel who have responsibility for purchasing, operating, maintaining and replacing power transformers.

FLUID DIAGNOSTICS SEMINAR
June 11, 2009

The Fluid Diagnostics Seminar will cover all aspects of dielectric fluid testing, maintenance and evaluation. Major topics include DGA for power transformers, LTCs, OCBs, Bushings, Oil Quality Assessment, Corrosive Sulfur and Natural Ester fluids.

Topics covered:

- Dissolved Gas Analysis (DGA) – Theory, Development, Condition Assessment and Applications for Power Transformers, LTCs, OCBs and Bushings
- Dielectric Fluid Quality and Acceptance Testing
- Dielectric Fluids, Mineral Oils and Natural Esters
- The Corrosive Sulfur Issue

Location: **Argonaut Hotel** - Fisherman's Wharf, SF

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www.weidmann-diagnostics.com

To arrange IEEE discount or seats for unemployed, please contact Sybil Jakob,
sybil.jakob@wicor.com 916-455-2284

Join the key experts in Mobile WIMAX and IMT-Advanced Technologies

IEEE Mobile WiMAX Symposium

July 9-10, 2009
Meritage Hotel, Napa Valley

43 technical papers in 10 sessions
2 Plenary Sessions
Held right before the IEEE 802 meetings in SF

MWS'09 addresses the technical challenges in mobile WiMAX and IMT-Advanced technologies. Attending will give good insights into the latest advancements in next-generation communication systems towards IMT-Advanced. This IEEE event is a platform for advanced knowledge of global research and implementations, and for meeting key experts from multiple disciplines leading the evolution of mobile communication technology. The conference features technical presentations on groundbreaking next-generation mobile communication technology, panel discussions, plus sessions reporting preliminary results and research-in-progress.

Sessions:

- Transmission Technology (I, II, III, IV)
- Networking Technology (I, II, III)
- Application and Service (I, II, III)

Keynote Talks:

- The Roadmap for Mobile Internet
- A Brief History of OFDMA and SC-FDMA
- Engineering Challenges in Field Deployment of 4G Wireless Broadband
- Non-trivial Applications of WiMAX: Dealing with Heterogeneous Requirements
- IEEE 802.16m for IMT-Advanced
-

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www.ieee-mobileWiMAX.org/2009

46th Design Automation Conference

Moscone Convention Center, SF July 26-31, 2009

Where The Electronic Design Community Meets…

DAC is the premier event for the design of electronic circuits and systems, and for EDA and silicon solutions. The DAC technical program is made up of tutorials, workshops, Pavilion panels and dozens of technical sessions divided into 12 Topical Areas, plus keynotes, panels, and over 200 exhibits.

Keynote Speakers:

Overcoming the New Design Complexity Barrier: Alignment of Technology and Business Models, Fu-Chieh Hsu - VP, Design & Technology Platform, TSMC

The End of Denial Architecture and the Rise of Throughput Computing, William J. Dally - Chief Scientist and Sr VP Research, NVIDIA & Stanford Univ

The Future for EDA: The CEO View, with **Aart de Geus** - CEO and Chairman of the Board, Synopsys, Inc., **Walden C. Rhines** - CEO and Chairman of the Board, Mentor Graphics Corp., and **Lip-Bu Tan** - President and CEO, Cadence Design Systems, Inc.

46th DAC Workshops (Sunday and Monday)

• Multiprocessor System-On-Chip: Current Trends and the Future • Moving from Traditional to Equation-Based DRC • 6th UML-SOC Workshop • Meeting the Challenges of ESD/ERC in a Mixed-Signal World • International Workshop on Bio-Design Automation • Young Faculty Workshop • Workshop for Women in Design Automation • Virtual Platform Workshop at DAC (Wed.)

Colocated Events:

- International Workshop on SLIP
- NASA/ESA Conference on AHS 2009
- Microelectronic Systems Education
- 2nd IEEE International Workshop on HOST
- 7th IEEE Symposium on Application Specific Processors
- IEEE/ACM Symposium on Nanoscale Architectures
- 3rd IEEE International Workshop on DFM&Y 2009
- North American SystemC Users Group
- Low-Power Coalition Workshop
- DFM Workshop - DFM Challenges at Sub-45nm Design
- Design Automation Summer School 2009

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- Over 50 research paper sessions arranged in six parallel tracks
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Sessions: (partial listing)

• Static Timing Analysis • Novel Design and Verification Methodologies • Design and Optimization of Nanocircuits • Statistical Methods in Static Timing Analysis • Low-Power Design and Analysis Techniques • Design Integrity Challenges • Optimized Embedded Software and MPSOCs • Advances in Embedded System Modeling and Optimization • Routing: From Chip to Package • Analog/RF Simulation and Statistical Modeling • Advances in Timing, ECO and Logic Optimization • Advances in Physical Synthesis • Thermal Optimization • Layout-Based Variability Modeling and Optimization • Advances in Core Verification Techniques • Robust Analog System Design • Embedded System Design for Low Power • Hardware Authentication, Characterization and Trusted Design • Targeted Test and Diagnosis • Parasitic Extraction in the Face of Process Variability • Network-On-Chip Advances for Power, Reliability and the Memory Bottleneck • Leveraging Parallelism in FPGAs and Multicore Systems • Heuristic Approaches to Hardware Optimization • Model Order Reduction Techniques and Applications

Tutorials:

• Low-Power SOC Design: State of the Art and Directions • High-Level Synthesis for ESL Design: Fundamentals and Case Studies • Post-Silicon Validation and Runtime Verification: Ensuring Correctness after First Silicon • CAD: Utilizing the State of the Art, and Beyond, in Parallel Programming • From Nanodevices to Nanosystems: Promises and Challenges of IC Design with Nanomaterials • Functional Verification Planning and Management: Navigating from Specification to Functional Closure

Advance Registration rates through June 29

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Renewable Energy, Introduction
Jun 18-Aug 20, Thu 6:30PM to 9:30PM, Cpto Campus
solar, wind, biomass, hydro, ocean (tidal, wave),geothermal…

Crosstalk & Static Noise Analysis using Primetime-SI
Jun 20-Jul 25, Sat 9:00AM to 2:00PM, Cupertino Campus
Models, timing analysis, reliability, nano-scale technology node, test cases, violations, hands-on lab course….

Storage Networking Design and Architecture
Jun 23-Aug 25, Tue 6:30PM to 9:30PM, Cpto Campus
SAN, NAS networking architectures, performance, best practices, replication, standards, management ….

Developing Applications for iPhone and iPod Touch
Jun 24-Jul 22, Wed 6:30PM to 9:30PM, Cpto Campus
SDK, Cocoa methodologies, Objective-C, iPhone OS ….

Designing with Xilinx FPGAs, Comprehensive
Jun 24-Aug 26, Wed 6:30PM to 9:30PM, Cpto Campus
resources, constraints, debugging, low-power, bottlenecks, hot-spots, clocks, design project, with Spartan 3A Starter Kit ….

Game Design and Production Overview
Jul 11-Aug 29, Sat 9:00AM to 12:00PM, Cpto Campus
concept, art assets, game engine, testing, producing, campaign add-on module for the game Neverwinter Nights 2….

Server Virtualization
Jul 20-Aug 17, Mon 6:30PM to 9:30PM, Cpto Campus
reduced energy, hardware partitioning, hypervisor, common servers, memory management, virtualized IO, network stack, shifting workload, managing guests, real-world usage….

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Register by June 7
Students may continue to register until June 15.

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- Session II - 5-week classes (June 15 - July 17)
- Session III - 5-week classes (July 27 - August 28)

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Review summer Open University courses:

www.scu.edu/engineering/graduate

IEEE Professional Skills Courses

SCV Chapters, Technology Management & Components, Packaging and Manufacturing Technology Societies

Presentation Skills for Engineers
- Date/Time: Tues, June 9, 8:30AM-4:30PM
- Location: Brocade, San Jose
- Fee: $500 for IEEE Members; $550 non-members

This class is top notch! Peter is very experienced and provided me with lots of good tips I can use on all my presentations. Definitely worthwhile.
-TIBCO Software

Clear Business, Technical, and E-Mail Writing
- Date/Time: Wed, June 17, 8:30AM – 12:30 PM
- Location: – Informatica, Redwood City
- Fee: $300 for IEEE Members; $350 non-members

Very practical and can use all lessons immediately in real life. -Cisco, Manager

Breakthrough Project Management
- Date/Time: Tues-Wed, Aug 18-19, 8:30AM-4:30PM
- Location: Synopsys, Mountain View
- Fee: $625 for IEEE Members; $700 non-members

This 2-day course provides participants with a common methodology, terminology and tools that produce more efficient results and increased buy-in through improved visibility, reliability and consistency.

Improve your skills – register for one of these classes, or for others coming up this spring. Bring a team!

Management Essentials
- Date/Time: Th/Fri, June 4-5, 8:30AM – 4:30PM
- Location: – Blue Coat Systems, Sunnyvale
- Fee: $625 for IEEE Members; $700 non-members

"Thank you!! I wish I could have had this knowledge a long time ago when I first became a supervisor."
-Sales Operations Supervisor, @Road

Transitioning from Individual Contributor to Manager
- Date/Time: Monday, June 8, 8:30AM-4:30PM
- Instructor Andrew Oravets
- Location: Cypress Semiconductor, San Jose
- Fee: $400 for IEEE Members; $500 non-members

"Excellent! The instructor's experiences have clearly demonstrated direction and path I would like to experiment with. This class was very clear and concise"

For complete course information, schedule, and registration form, see our website:

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FLASH MEMORY SUMMIT

August 11-13, 2009
Santa Clara Convention Center

- Tutorials - Exhibits - Sessions

This power-packed 3-day event will cover the latest topics in flash memory. Hear about flash in embedded systems, laptop design, flash in enterprise storage systems, green flash, solid state drives, flash performance, flash-based design, flash in computers, mobile applications, software, new non-volatile memory technologies, reliability, security, and much more!

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- The Many Flavors of NAND…and More to Come
… and more

FORUM and SESSION TOPICS:

- Flash Memory in Embedded Systems - Flash Memory-Based Architectures - Enterprise Storage Systems - Solid State Drives (SSDs) - Flash Performance - Data Center Applications - History of Flash Memory - Consumer Applications - Security - Life Beyond Flash: New Non-Volatile Memory - System and Controller Design (error correcting codes) - Market Research - NOR Flash - Flash Testing and Reliability - Executive Updates: Power in IT; CIOs and Corporate Laptops

For the full program, please visit:

www.flashmemorysummit.com

Save $100 – use priority code "IEEE"

The ASME Nanotechnology Institute, in cooperation with the IEEE's Engineering in Medicine and Biology Society, is pleased to announce the 2nd Frontiers in Biomedical Devices conference, to be held June 7-8 in Irvine. Leading authorities in the commercial and academic arenas will focus their expertise in nine technical tracks plus posters:

- Imaging & Monitoring the Environment
- Simulation & Modeling
- Device Testing
- Bio-Sensors & Diagnostics
- Device Design & Development
- Therapeutic Devices
- Next Generation Device Technology
- Clinical & Regulatory
- Posters / Student Posters

Our program will be co-chaired by **Abe Lee, Ph.D.** of the University of California's Henry Samueli School of Engineering's Biomedical Engineering Department, and co-chaired by **Walt Baxter, Ph.D.** of Medtronic Cardiac Rhythm Management.

ASME EMERGING TECHNOLOGIES

WHO SHOULD ATTEND

Medical device engineers, research scientists, government & academic personnel, and those involved in medical device research, discovery, clinical evaluation and delivery of medical devices are encouraged to attend.

The conference also includes an evening reception/ exhibition/poster session/panel session (with OCTANe) on June 7th at the hotel. Posters will be presented and displayed during the conference.

The **Hyatt Regency Irvine hotel** is conveniently located near the John Wayne Airport.

For more information and to register,

visit: **www.asmeconferences.org/biomed07**

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Contact Brandy Smith at smithb@asme.org
or 917-596-0306

InterPACK '09
July 19-23, 2009
Westin St. Francis
San Francisco

Conference and Exhibition on
Packaging and Integration of Electronic and Photonic Systems, MEMS, and NEMS

The **InterPACK '09 Conference** promotes international cooperation, understanding, and development of efforts and disciplines in Microelectronics, Photonics, Microwave, MEMS and NEMS Systems Packaging and Integration. Emerging knowledge, research results, new developments, and novel thermal, mechanical, electrical, and materials packaging product concepts in Electronic Packaging Engineering will be presented in unique forums.

Focus of InterPACK '09:

• Advanced Packaging • Electro-Thermal-Mechanical Issues in Packaging (Multi-Physics) • Materials and Processes • MEMS and MEMS Packaging • Manufacturing and Test • Modeling and Simulation • Nanotechnology and NEMS • Photonics and Optics • Reliability • Thermal Management • Emerging Technologies

Co-located with ASME Summer Heat Transfer Conference and ASME Energy Sustainability Conference

All registrations include **complimentary admission** to the InterPACK shortcourses/tutorials held on Sunday, July 19.

Early Registrations (by **June 15**) include a $100 banquet ticket. Save by registering early!

For full program and registration information:

www.interpackconference.org

Career Development Workshops from Consultants Network of Silicon Valley (CNSV) and SCV Section

Communication Tools for Consultants

Friday June 12, 2009
KeyPoint Credit Union, Santa Clara
8:30 AM thru 12:30 PM
$47 for IEEE members; $147 for non-members

As a consultant, your clients want your technical expertise, but they also want to work with you in a positive, productive, and amicable way. You must have good communication skills. Get even more successful than you already are by improving your communication skills, with Steven Cerri, trainer and coach. **Limited to the first 24.**

It has become clear to the successful consultant members in the IEEE-CNSV, that effective communication is critical to your success as a consultant. Here is your chance to be even more successful than you already are by improving your communication skills.

In this class, you will learn...

1. how to build natural rapport
2. how to connect with your potential clients so they feel comfortable with you
3. how to motivate your customer to tell you their actual needs and expectations
4. how to expand your client base beyond the "easy" clients to the rest of your potential base

RSVP: by **June 11** to get one of the available seats.

Visit **cnsv-communication.eventbrite.com**

Marketing Your Consulting Services On Craig's List

Saturday June 13, 2009
Cogswell College, Sunnyvale
8:30 AM thru 12:30 PM
$47 for IEEE members; $67 for non-members

Marketing on Craig's List should be near the top of any successful consultant's ToDo list. So here is your chance to get even more successful than you already are. Set up a "consulting resume presence" on Craig's List. Bring your laptop (with wireless capability) for step-by-step hands-on training. **Limited to first 24.**

This workshop is presented by Carl Angotti, a member of IEEE and CNSV. Carl is a successful consultant with over 25 years of consulting experience. He and other engineering consultants have used Craig's List to successfully market their services for several years and Carl has agreed to share his secrets. Expect to receive an email with a brief homework assignment. This will give you a jump-start on understanding the process.

RSVP: by **June 12** to get one of the available seats.

Visit: **cnsv-marketing-clist-egrid.eventbrite.com**

2009 Vancouver Workshop

CMOS Emerging Technologies Workshop

Theme: Research & Business Opportunities Ahead

September 23-25, 2009 Vancouver, BC, Canada

CMOS Emerging Technologies

The **CMOS Emerging Technologies Workshop** is a research and business event for those who want to discuss and discover new and exciting high tech opportunities. The format of the talks resembles in-depth tutorials describing state-of-the-art technology and future research directions rather than presenting specific research results or commercial products. The 6th annual workshop will be held downtown Vancouver with numerous opportunities for personal exploration of surrounding tourist attractions.

No formal proceedings will be printed but attendees will receive PDF copies of all presentation material. Selected and expanded workshop papers are edited as books with a number of the titles already published or in preparation – see the website.

Plenary Session Talks:

Prof. John Rogers, UI-UC, **Stretchable Si CMOS: From Electronic Eyeball Cameras to Conformal Brain Monitors**

Roberto Saracco, Senior Director, Telecom Italia Future Center, **Emerging Applications and Telecom Business Trends**

Sessions: *(see full Program on website)*

- Communications - Biomedical Circuits - Biomedical Engineering - Wireless - Nanotechnology/Nanoelectronics - Microsystems - RF Circuits - Mixed-Signal - I/O Circuits - Converter Circuits - Optical/Medical Imaging - Photonics - VLSI - SOC - Radiation Detectors/Imagers - Circuits for Radiation - Silicon Technology - Programmable Devices - EDA Design Tools - Business Development

Registration is now open! Plan to attend …

www.CMOSet.com*

9th Annual Computer Society Chapter Conference *2009 New Frontiers in Computing Technology*

Hand-Held Devices

July 18, 2009 (Saturday)
Bruan Auditorium, Stanford University

The marvels of hand held devices are emerging. Integrated with our lives are smart cell phones. In addition to voice communication, we use it to text message, to play games, and to search for information on the internet. Other valuable uses for hand held devices are to collect, store, and transmit data, such as the glucose meter, the cashier price meter, or the global position device. Revolutionizing our lives, hand held devices will be this year's topic in New Frontiers in Computing Conference (NFIC). The one-day conference has invited academia and professionals to speak on the hardware, the infrastructure, the software, the business models, and the social impacts. We encourage any interested person to come, to learn, and to network with others on the technology.

This year's one-day conference on emerging technology is aimed to providing an inexpensive, solid overview of a technology that may affect your work and career in the near future.

Registration is at 8:30AM; talks are between 9:00 AM and 4:00 PM

For more information, see:

www.ewh.ieee.org/r6/scv/computer

SCV Communications

SATURDAY May 30, 2009

Seminar: Mobile Broadband Ecosystem for the Pacific Rim

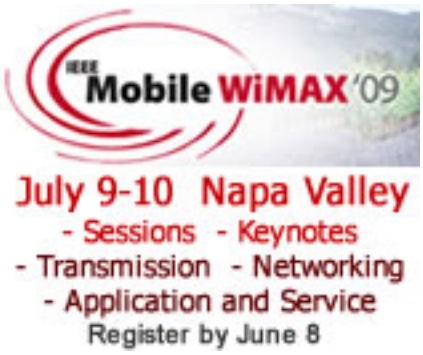
Speakers: from AT&T, CMCC Research, ZTE-USA, Huawei-USA, Treyspan, 3GPP RAN1
Time: 1:30 PM - 5:30 PM
Cost: IEEE Members and unemployed/students $10; non-members $30 (thru May 23)
Place: Daly Science Building, Room 206, Santa Clara University, 500 El Cameno Real, Santa Clara
RSVP: online, through ComSoc website
Web: www.ewh.ieee.org/r6/scv/comsoc

After the recent carrier restructuring and 3G license issuing in China, the markets in the Pacific Rim including US, China, Japan and others, ahve become a unique place in the world, where all major 3G and other wireless broadband technologies are demonstrating themselves and compete against each other. At the same time, moving to the 4G era in major metropolitan areas hits up the debate between WiMAX and LTE. In this diversified wireless network environment, the wireless network equipment vendors and handset manufacturers are facing tremendous challenges as well as opportunities. What is the future trend of wireless broadband development in those major markets? What lessons can they learn from each other in US, Greater China, Japan and other areas?

Through theis series of presentations and a panel discussion, you will meet the speakers from different sectors in the wireless industry around the Pacific Rim, who will have the insight and knowledge to answer all your questions.

1:30 - 1:50pm Registration
1:50 - 2:00pm Welcome
2:00 - 2:20pm Dr. Dawei Zhang, Director of Wireless Research, CMCC Research
2:20 - 2:40pm Chris Boyer, VP, AT&T
2:30 - 3:00pm Rongqin Yan, VP Product Development,ZTE USA
3:00 - 3:20pm Dr. Steve Gray, CTO and Corp VP, Huawei USA
3:20 - 3:40pm Dr. William Lee, Chairman, Treyspan
3:40 - 4:00pm Sadayuki Abeta, Vice Chair, 3GPP RAN1
4:00 - 4:20pm Break
4:20 - 5:00pm Panel Discusion
5:00 - 5:20pm Q&A Moderator: Derek Kerton, Principal Analyst, Kerton Group
5:40pm Adjourn

Early Registration (by May 23rd)		On-site Registration
SVCW or IEEE Member	$10	$30
Student / Unemployed	$10	$30
SVC W Associate Member	$30	$50
Non Member	$30	$50



SCV Photonics (Lasers and Electro Optics)

TUESDAY June 2, 2009

Where in the Nano-world is Lithography Taking Us?

Speaker: Dr. Harry J. Levinson, GLOBALFOUNDRIES
Time: Networking/Pizza at 6:00 PM, Presentation at 7:00 PM
Cost: none
Place: National Semiconductor Building E Auditorium, 2900 Semiconductor Drive, Santa Clara
RSVP: use web link for EventBrite
Web: www.ewh.ieee.org/r6/scv/leos

For decades, patterns of integrated circuits have been fabricated using optical lithography using near- to deep-ultraviolet light. However, this method is approaching fundamental physical limits, in terms of the ability to print dense patterns directly. The reasons for this are described, and the outlook for some of the alternatives currently being serious consideration, such as double patterning and extreme ultraviolet (EUV) lithography, are discussed. Included in the discussion will be economic as well as technical issues.

Harry J. Levinson is a Sr. Fellow and manager of GLOBALFOUNDRIES's Strategic Lithography Technology Department, which is responsible for advanced lithographic processes and equipment. Dr. Levinson started his career in Bipolar Memory Development at AMD, then spent some time at Sierra Semiconductor and IBM, before returning to AMD - now GLOBALFOUNDRIES - in 1994. During the course of his career, Dr. Levinson has applied lithography to many different technologies, including bipolar memories, 64Mb and 256Mb DRAM development, the manufacturing of applications-specific integrated circuits, thin film heads for magnetic recording, flash memories and advanced logic. He was one of the first users of 5 steppers in Silicon Valley and was an early participant in 248 nm and 193 nm lithography. Dr. Levinson also served for several years as the chairman of the USA Lithography Technology Working Group that participates in the generation of the lithography chapter of the International Technology Roadmap for Semiconductors. He has published numerous articles on lithographic science, on topics ranging from thin film optical effects and metrics for imaging, to overlay and process control, and he is the author of two books, **Lithography Process Control** and **Principles of Lithography**. He holds over 40 US patents. Dr. Levinson is an SPIE Fellow and chairs the SPIE Publications Committee. He has a BS in engineering from Cornell University and a PhD in Physics from the University of Pennsylvania.

THURSDAY June 4, 2009

ELECTRIC: a Multithreaded Integrated-Circuit Design System

Speaker: Dr. Steven M. Rubin, Sun Labs
Time: Networking and food at 6:00 PM, Presentation at 7:00 PM
Cost: none ($2 for parking)
Place: UC Santa Cruz, Room 180, Engineering Bldg 2, Santa Cruz
RSVP: by email to Marcelo Siero, siero@ee.com
Web: www.ee.com/electric

Steven M. Rubin is the author of the Electric VLSI Design System, and the CAD tools textbook "Computer Aids for VLSI Design." He received his doctorate at Carnegie Mellon University and has done research at Bell Labs, Schlumberger, Apple Computer, Interval Research, and Sun Microsystems. Specializing in visually-oriented computing, his research has spanned computer vision, graphics, and CAD. Steve was also the lead singer of Severe Tire Damage, the first band to perform live on the Internet.

The Electric VLSI Design System is an open-source circuit-design system that has been used for decades to make integrated circuit (IC) chips. Written in 1982, it predates most commercial circuit design systems available today. Beginning in 2003, a small team at Sun Microsystems translated Electric from C to Java, completing the task in less than two years. The resulting system is more stable, has an improved user interface, and (to the surprise of many) is faster.

One of the reasons for the new translation was to take advantage of Java's powerful multithreading facilities. While attempting to make use of these facilities, it was determined that a thread-safe database was needed. We split the system into a database server and a user-interface client. This new database has a number of advantages, including: collaborative design, thin-client design terminals, reliable crash recovery, reduced memory usage, and the ability to use multiple processors.

This talk describes these improvements to Electric and describes two multithreading facilities that have been built: a design-rule checker (DRC) and a wire router.

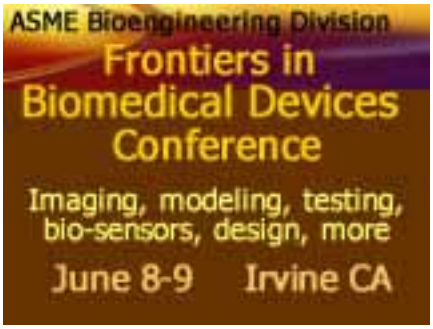
SCV Technology Management

THURSDAY June 4, 2009

Goldilocks and the Three Bears: Two Case Studies of Optimal Development Processes for Startups, Large Companies

Speaker: John Carter, Principal, TCGen Inc.
Time: Guided Networking at 6:30 PM, Sandwiches/drinks at 7:15 PM, Presentation at 7:45 PM
Cost: $10 (IEEE member), $13 (non member) (add $3 without reservation)
Place: Ramada Inn, 1217 Wildwood Ave, Sunnyvale
RSVP: through the website
Web: www.ieee-scv-ems.org

John Carter has been a CEO, founder, and a widely respected advisor to technology firms over his thirty year career. He has advised M&A strategies for many technology firms as Principal of TCGen Inc. In this capacity he has raised private equity and assumed roles of CEO and CTO (Livescribe, Klipsch). Prior to TCGen, he was the founder and a Principal of Boston-based Product Development Consulting, Inc., a leading organization advising Fortune 500 companies in the areas of research, development, and marketing. He has consulted to high technology companies, including clients such as Apple, Cisco, HP, IBM, and 3M. Before starting PDC, John was Chief Engineer of BOSE Corporation. He earned his SM in electrical engineering from MIT and a BS in engineering from Harvey Mudd College in Claremont, CA.



How much process is just right for a rapidly scaling software development organization? Too much process can stifle creativity and slow down development, resulting in products that miss the market. Too little process often results in changing definition, team confusion and resource misalignment, resulting in delays in time to market. In a little over 90 days a product development process was implemented in a startup organization of approximately 100 people that resulted in programs that beat their schedule estimates. This was achieved by a philosophy of "inch wide, mile deep' implementation of only three key elements, that if implemented well are necessary and sufficient to drive fast cycle time: Simplified Product Definition, Consensus driven cross functional schedule, and Concept Management Review. And a single management metric – Behavioral Change – which supports the implementation of this methodology so one tangibly can see the behavioral change. Nothing else. Nada.

The presentation will describe the case study of the implementation of these best practices, how the organization actually liked and leveraged the process, and the beneficial impact of the results. But this work is not just for start-ups – a contrast will be provided of a successful implementation of the same methodology for an organization of 6,000 engineers. Specific examples of the metrics and deliverables will be presented, and attendees will gain knowledge that they can immediately begin implementing in their companies.

Guided Networking – Product Development Process – too much, too little

Attendees are encouraged to think about the night's theme – the process of product development projects. We'll discuss examples from attendees experiences. In the process get to know fellow meeting attendees.

June 7 thru June 11, 2009

IEEE Stationary Battery Technical Committee Meetings

Activity: TC Meetings all week; two Tutorials on Sunday afternoon
Time: See agenda, posted on website, for which days are of interest to you
Cost: hotel charge is $73/day for meals (for those commuting); $100 more gets you a room plus meals
Place: Doubletree Hotel Sonoma Wine Country, 1 Doubletree Drive, Rohnert Park
RSVP: Interested IEEE members and non-Members may register through the website
Web: www.ewh.ieee.org/cmte/PES-SBC/next_meeting.htm

Our locale is hosting the IEEE Stationary Battery Technical Committee, Summer 2009 meeting in Rohnert Park from June 7 – 11, 2009. This committee writes the following standards:

IEEE 450 - Vented Lead-Acid Maintenance & Testing
IEEE 1188 - VRLA Maintenance & Testing
IEEE 484 - Vented Lead-Acid Battery Installation
IEEE 1189 - VRLA Battery Selection
IEEE 485 - Vented Lead-Acid Battery Sizing
IEEE 1375 - Battery Protection
IEEE 535 - Nuclear Battery Qualification
IEEE 1491 - Battery Monitoring
IEEE 1106 - Ni-Cd Installation, Maintenance & Testing
IEEE 1578 - Battery Spill Containment
IEEE 1115 - Ni-Cd Battery Sizing
IEEE 1625 - Battery; Portable Computing
IEEE 1184 - UPS Batteries
IEEE 1725 - Cell Phone Batteries
IEEE 1187 - VRLA Installation
PAR 1657 - Battery Technician Qualification
PAR 1660 - Application & Management of Stationary Batteries used in Cycling Service
PAR 1635 - Battery Ventilation & Thermal Management
PAR 1679 - Recommended Practice for the Characterization and Evaluation of Emerging Battery Technologies in Stationary Applications
PAR 1825 - Rechargeable Batteries for Digital Cameras and Camcorders

Guest (IEEE members and non-members) are welcome to attend all or a portion of the meeting. The meeting agenda will be posted on the website.

Note: The hotel will charge a daily fee of $73 to cover breakfast, lunch, breaks and meeting room services to any “Non-Group Block” guest (ie, not staying in the hotel).

Kindly RSVP if you plan to attend, to:
Mike Jump , WG Chair – IEEE 1187
mike.jump@rbc.com

SCV Electron Devices

TUESDAY June 9, 2009

Negative Bias Temperature Instability in p-MOSFETs: Fundamentals, Characterization, Materials Dependence and Modeling

Speaker: Dr. Souvik Mahapatra, Dept. of Electrical Engineering, IIT Bombay
Time: Social/pizza at 6:00 PM, Presentation at 6:15 PM
Cost: none
Place: National Semiconductor, Building E1, Conference Center, 2900 Semiconductor Dr, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds

Souvik Mahapatra received his Ph.D. in Electrical Engineering from Indian Institute of Technology, Bombay (IITB), India in 1999. From 2000 to 2001 he was at Bell Laboratories, Lucent Technologies, Murray Hill, NJ. Since 2002 he is with the Department of Electrical Engineering, IITB, where he is presently a Professor. He is also an Adjunct Professor of ECE Department at Purdue University. His research interests are electrical characterization of defects in dielectric-semiconductor interfaces; hot-carrier and bias temperature instability in CMOS devices; high-k and novel dielectrics for CMOS; and Flash EEPROMs. He has published more than 85 papers in refereed international journals and conferences, was invited to speak at several major international conferences including the IEDM, was a tutorial presenter at IRPS and has worked as a reviewer for many international journals and conferences. Dr. Mahapatra is an IEEE Electron Device Society Distinguished Lecturer.

Negative Bias Temperature Instability (NBTI), causing shifts in device parameters such as drain current and threshold voltage, is a serious reliability concern for p-MOSFETs. Though identified more than 40 years ago, NBTI has become the most severe front-end reliability issue only recently, as gate oxide thickness is scaled below 2nm, and Nitrogen is incorporated into the gate oxide to prevent Boron penetration and leakage. Besides Si oxynitride/poly-Si devices, NBTI is also a serious concern for high-k/metal gate devices as well.

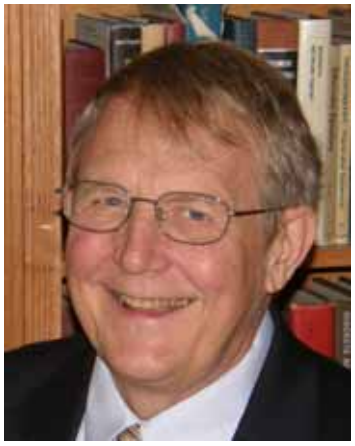
Like other reliability issues (such as HCI), device lifetime under NBTI is determined by accelerated stress tests done at short times, and extrapolating the degradation under operating conditions to end of life. It is very important to choose proper stress conditions such that defects responsible for NBTI are only accelerated and no new defects are formed. As NBTI degradation recovers (unlike HCI) after stress is turned off for measurement, conventional stress-measure-stress methods give erroneous results, and fast methods must be implemented. It is important to understand and model the NBTI physical mechanism, so that proper physics-based models can be developed for reliable determination of device lifetime. It is also important to understand the process/material dependence of NBTI to develop robust, NBTI-safe gate insulators that meet other (leakage, mobility) requirements. The talk will address some of these issues.

TUESDAY June 9, 2009

The Life of SPICE

Speaker:	Laurence Nagel, Omega Enterprises Consulting (and originator of SPICE)
Time:	Social at 5:30 PM, dinner at 6:30 PM, Presentation at 7:30 PM
Cost:	$24 for dinner and presentation
Place:	Del Monte Restaurant, 100 South Murphy Avenue, Sunnyvale
RSVP:	From website, use PayPal. Alternately, you can mail a check and send an email RSVP to Brian Berg, brianberg@gmail.com
Web:	www.CaliforniaConsultants.org

Laurence W. Nagel has worked in the IC industry for more than 40 years. He developed the SPICE circuit simulation program while earning his BS, MS, and PhD degrees at UC Berkeley. Larry then began a 20 year career at Bell Laboratories which included developing the ADVICE circuit simulation program; participating in the development of the Kull-Nagel bipolar model; designing analog circuits for submicron NMOS processes; working in the AT&T Intellectual Property Division on assertion of patents and negotiation of patent licenses; and serving as project manager in the development of the Celerity circuit simulation program.



Dr. Nagel then joined Anadigics, Inc., where he managed simulation of RF integrated circuits; modeling and characterization of GaAs MESFET device processes; and importing silicon CMOS design tools and foundry support. In 1998, he founded Omega Enterprises Consulting, through which he offers services in analog and RF integrated circuit design, device modeling, circuit simulation, and expert witness work in patent and trade secret litigation. Larry is an IEEE Fellow.

While the integrated circuit industry thrives on constant change and new technology, the SPICE circuit simulation program has been around the industry for almost forty years. As a result, many engineers who make use of this software weren't even born when Larry Nagel released its first version.

This talk will chronicle the journey of SPICE since the late 1960s: its origins as a teaching program at UC Berkeley, its spread into industry, and its creation of a cottage industry that supports and expands the variants of "alphabet SPICE." Dr. Nagel will credit the various contributors to this saga while sharing a bounty of amusing stories.

Larry will also speculate on how this particular program has evolved while staying pretty much the same, a claim that likely no other computer program can make.

SF Communications

TUESDAY June 9, 2009

Internet 2.0: Hype or Hope?

Speaker: Prof. Henning Schulzrinne, Columbia University
Time: 6:30 PM
Cost: none
Place: California PUC Building, 505 Van Ness Ave, San Francisco
RSVP: by email to Tim Ryan, timryan@ieee.org
Web: www.ieee.org/sfcomsoc

Prof. Henning Schulzrinne received degrees from Darmstadt (Germany) University of Technology, the University of Cincinnati and the University of Massachusetts in Amherst. He has held research positions at GMD Fokus, Berlin and Bell Laboratories before joining the faculty of Columbia University, New York. He is currently chairing the Department of Computer Science. His research interests encompass real-time network services, ubiquitous and mobile computing and network reliability. He is a co-author of more than 50 RFCs, including RTP, RTSP, SIP and GIST.

The Internet has become a core civilizational infrastructure, along with energy, water and transportation. However, there are increasing concerns that the current design of the Internet has ossified, yielding ever more complex systems that remain unreliable. I will try to outline some of the key challenges facing the Internet, from address exhaustion, routing scaling and fairness to security and manageability, and summarize some of the research and early standardization efforts that try to address these problems.

WEDNESDAY June 10, 2009

Wafer-Level Packaging – Next Turn in the Road

Speaker: Dr. Thomas Di Stefano
Time: Optional dinner at 6:30 PM; Presentation at 7:30 PM
Cost: $25 if reserved by June 8; $30 at door (no cost for presentation)
Place: Biltmore Hotel, 2151 Laurelwood Rd (Fwy 101 at Montague Expressway), Santa Clara
RSVP: via the DoubleKnot registration page, from website
Web: www.cpmt.org/scv

Dr. Tom Di Stefano is President of Centipede Systems, a technology based company dedicated to providing MicroConnectors and contactors at the highest levels of density and performance. Prior to Centipede, Tom was the founding President of Tessera, ranked in the top ten hot growth companies by Business Week 2005. He is also a co-founder of ***Chip Scale Review***, a leading magazine in microelectronics technology. Tom is an industry veteran with 19 years of experience at IBM Watson Laboratories. At IBM, he was a member of the IBM Academy of Technology. Tom earned a PhD from Stanford University and BSEE with Highest Honors from Lehigh University. He is an author of more than 220 US Patents and numerous publications in science and technology.

Wafer Level Packaging has long been the promised land of semiconductor manufacturing, but to many it seems we are still in the wilderness. The promise is as attractive as ever and even more so in an economic environment where continuous cost reduction dictates rationalization of back-end packaging and test. Until now, Wafer Level Packaging has proceeded slowly into larger, high-value devices where a reliable die attach technology is an ongoing issue. Presently, several DRAM manufacturers are readying Wafer Level or Through Silicon Via packaging for production. This next leg upward will require cost-effective infrastructure for burn-in, test and handling. The methods, tools and standards necessary for growth of this supporting infrastructure represent both a problem and an opportunity. It is not at all clear which of several alternative paradigms will win, but one thing is sure -- the back-end infrastructure needs attention and coordinated effort, and perhaps new paradigms for solving long-standing problems known earlier under the rubric "KGD".

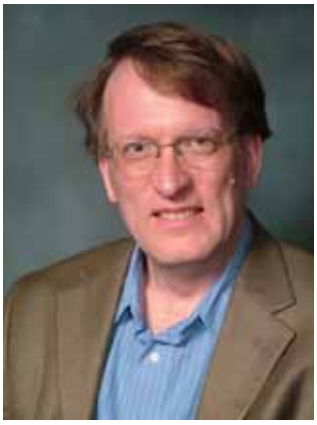
WEDNESDAY June 10, 2009

Distinguished Lecture:

VoIP for Wireless

Speaker: Prof. Henning Schulzrinne, Columbia University
Time: Networking/Pizza at 6:00 PM, Presentation at 6:30 PM
Cost: none
Place: National Semiconductor Building E, Conference Room, 2900 Semiconductor Drive, Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/comsoc

IEEE 802.11-based networks are likely to become popular as replacements for cordless phones, particularly in enterprise settings, and as a way to fill in cellular coverage inside buildings and homes. However, using 802.11a/b/g for VoIP poses a number of challenges, including how to make hand-offs transparent, how to maximize capacity and how to limit the number of concurrent calls to avoid quality degradation. In the IRT Lab at Columbia University, we have proposed and investigated a number of techniques that address these issues. In addition, measurements of 802.11 networks illustrate some of the operational and modeling challenges.



This is joint work with Ashutosh Dutta, Andrea Forte, Sangho Shin and Kenta Yasukawa.

Prof. Henning Schulzrinne received his undergraduate degree in economics and electrical engineering from the Darmstadt University of Technology, Germany, his MSEE degree as a Fulbright scholar from the University of Cincinnati, Ohio and his Ph.D. degree from the University of Massachusetts in Amherst, Massachusetts. He was a member of technical staff at AT&T Bell Laboratories, Murray Hill and an associate department head at GMD-Fokus (Berlin), before joining the Computer Science and Electrical Engineering departments at Columbia University, New York. He is currently chair of the Department of Computer Science.

He is editor of the "Computer Communications Journals", the "ACM Transactions on Multimedia Computing", the "ComSoc Surveys & Tutorials" and the "IEEE Internet Computing Magazine", and a former editor of the "IEEE Transactions on Image Processing", "Journal of Communications and Networks" and "IEEE/ACM Transactions on Networking".

He has been a member of the Board of Governors of the IEEE Communications Society and is vice chair of ACM SIGCOMM, former chair of the IEEE Communications Society Technical Committees on Computer Communications and the Internet and has been technical program chair of Global Internet, IEEE Infocom, NOSSDAV, IM, IFIP Networking 2009 and IPtel and General Co-Chair of ACM Multimedia 2004 and ICNP 2009. He serves on the Internet2 Applications, Middleware and Services Advisory Council and as working group chair in the NSF GENI project. He also has been a member of the IAB (Internet Architecture Board). He serves on a number of conference and journal steering committees, including for the IEEE/ACM Transactions on Networking.

Protocols co-developed by him, such as RTP, RTSP and SIP, are now Internet standards, used by almost all Internet telephony and multimedia applications. His research interests include Internet multimedia systems, quality of service, and performance evaluation.

He served as Chief Scientist for FirstHand Technologies and Chief Scientific Advisor for Ubiquity Software Corporation. He is a Fellow of the IEEE, has received the New York City Mayor's Award for Excellence in Science and Technology, the VON Pioneer Award and the TCCC service award.

SCV Robotics and Automation

THURSDAY June 11, 2009

Modular Robotics Technologies: Sculpting Behavior

Speaker: Hayes Raffle, Nokia Research Center
Time: Presentation at 7:00 PM
Cost: none
Place: Carnegie Mellon Silicon Valley, NASA Research Park, Bldg. 23, Moffett Field
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/ras

Hayes Raffle is an award-winning product designer and inventor specializing in hybrid physical/digital objects to nurture learning, creative expression, and interpersonal communication. He is currently at Nokia Research Center, Palo Alto where he is inventing new technologies to support family communication.

Hayes completed his Ph.D. in the Tangible Media Group a the MIT Media Lab in June, 2008 and received his M.S. from MIT in 2004. His research integrates design, epistemology and human-computer interaction, with a focus on educational toys. Hayes was a LEGO Fellow for six consecutive terms and researched new technologies for hands-on learning. Major projects include the Topobo robotic construction kit, Super Cilia Skin textural communication medium, Jabberstamp drawing tools, and Fuzzmail emotional email application. Hayes's inventions have received numerous international awards and recognition, and have shown in Europe, Asia and North America. His work has received outstanding press from major publications including the New York Times, Wall Street Journal, and BBC. Hayes is the author of several patents and over a dozen peer-reviewed academic publications.

Outside of the Media Lab, Hayes has done industrial design for IDEO Palo Alto, and has run the Rafelandia design consultancy in Boston and San Francisco serving diverse clients including SONY and Leapfrog Toys. While completing his B.A. in Fine Arts from Yale University, Hayes helped design and develop the award-winning ZOOB® building toy and later helped to found Primordial, LLC to market, manufacture and sell ZOOB internationally. He is currently bringing Topobo toys to market as principal of Topobo, LLC.

For over a century, educators and constructivist theorists have argued that children learn by actively forming and testing – constructing – theories about how the world works. Recent efforts in the design of "tangible user interfaces" (TUIs) for learning have sought to bring together interaction models like direct manipulation and pedagogical frameworks like constructivism to make new, often complex, ideas salient for young children. Tangible interfaces attempt to eliminate the distance between the computational and physical world by making behavior directly manipulable with one's hands. In the past, systems for children to model behavior have been either intuitive-but-simple, e.g. curlybot or complex-but-abstract, e.g. LEGO Mindstorms. In order to develop a system that supports a user's transition from intuitive-but-simple constructions to constructions that are complex-but-abstract, I draw upon constructivist educational theories, particularly Bruner's theories of how learning progresses through enactive then iconic and then symbolic representations.

I present the Topobo system, a class of tools that helps people transition from simple-but-intuitive exploration to abstract-and-flexible exploration. The system is designed to facilitate mental transitions between different representations of ideas, and between different tools. A modular design approach, with an inherent grammar, helps people make such transitions. With Topobo, children use enactive knowledge, e.g. knowing how to walk, as the intellectual basis to understand a scientific domain, e.g. engineering and robot locomotion. Queens, backpacks, Remix and Robo add various abstractions to the system, and extend the tangible interface. Children use Topobo to transition from hands-on knowledge to theories that can be tested and reformulated, employing a combination of enactive, iconic and symbolic representations of ideas.

OEB Industry Applications

THURSDAY June 11, 2009

Motor Design Considerations for Above-NEMA AC Induction Motors

Speakers: Ben Flick and Scott Kreitzer, Siemens Energy and Automation
Time: Social at 5:30 PM; Presentation at 6:15 PM; Dinner at 7:15 PM; Presentation continues at 8:00 PM
Cost: $20 for IEEE members; $25 for non-members
Place: Marie Callender's Restaurant - The Garden Room, 2090 Diamond Blvd (near the Concord Hilton Hotel), Concord
RSVP: by June 10, by email to Gregg Boltz, gboltz@brwncald.com, (925) 210-2571
Web: www.ewh.ieee.org/r6/scv/ras

Above NEMA motor frames are larger than standard NEMA. They typically range from 200 to 10,000 HP and are constructed to meet the specific requirements of an application.

This presentation will focus on the following key areas:

- Above NEMA Motor Electrical Design Techniques
- Above NEMA Motor Mechanical Design Techniques
- Testing for Above NEMA Motors
- IEEE and API Standards

Benjamin D. Flick received his BS degree in Electrical Engineering from the University of Cincinnati, Ohio. Currently, he is Manager, Product Engineering for Siemens Energy & Automation Power Conversion Division Above-NEMA motor facility in Norwood, Ohio. He is active in NEMA working groups.

Scott Kreitzer graduated with a BSME degree from Wright State University in 1993 and received a Master of Science degree in Aerospace Engineering from the University of Cincinnati in 1995. Scott worked for Reuland Electric in 1994 as a Design Engineer developing high-speed AC induction motors. He is currently the Manager of Engineering in the Above NEMA motor development group at Siemens Energy and Automation. Scott is an associate member of IEEE.

SCV Consultants' Network of Silicon Valley with SCV Section

FRIDAY June 12, 2009

Communication Tools for Consultants

Instructor: Steven Cerri, engineer, consultant, trainer and coach
Time: 8:30 AM thru 12:30 PM (no lunch)
Cost: $47 for IEEE members; $147 for non-members
Place: KeyPoint Credit Union, 2805 Bowers Ave., Santa Clara
RSVP: by June 11, on EventBrite site cnsv-communication-egrid.eventbrite.com; limited to 24
Web: cnsv-communication-egrid.eventbrite.com

Whether you are...

1. reaching out to a potential customer
2. negotiating a contract
3. defining requirements
4. delivering products
5. getting paid

…the better your communication skills, the greater your success.

As a consultant, you often believe that you are hired primarily for your technical expertise. But actually it's more complicated than that. Your clients do indeed want your technical expertise, but they also want to work with you in a positive, productive, and amicable way. That means you must have good communication skills. It means that you have to connect with your customers on a level that builds rapport.

And it's become clear to the successful consultant members in IEEE-Consultants Network of Silicon Valley (CNSV) that effective communication is critical to your success as a consultant. That's why they are co-sponsoring this event. Here is your chance to get even more successful than you already are by improving your communication skills.

Join Steven Cerri, engineer, consultant, trainer and coach to engineers, on June 12 at KeyPoint Credit Union, for a morning of communication training.

In this class, you will learn...

1. how to build natural rapport
2. how to connect with your potential clients so they feel comfortable with you
3. how to motivate your customer to tell you their actual needs and expectations
4. how to expand your client base beyond the "easy" clients to the rest of your potential base

The workshop will be held at the KeyPoint Credit Union (2805 Bowers Ave., Santa Clara), and laptops are not required.

Notes:

1. This workshop registration ends at midnight on June 11, 2009. Sorry, no walk-ins.
2. This workshop is limited to 24 people to enhance interactivity.
3. Arrive a little before 8:30AM and register, enjoy complimentary coffee and bagels, and be prepared to advance your business!
4. Lunch will not be provided and the workshop will end promptly at 12:30PM.

This seminar is part of a series organized by CNSV to help its members advance their skills during these difficult times.

This event is being co-sponsored by the Santa Clara Valley Section of IEEE and the IEEE-Consultants Network of Silicon Valley (IEEE-CNSV).

SATURDAY June 13, 2009

Marketing Your Consulting Services On Craig's List

Instructor: Carl Angotti, CNSV member and consultant
Time: 8:30 AM thru 12:30 PM (no lunch)
Cost: $47 for IEEE members; $67 for non-members
Place: Cogswell Polytechnic College, 1175 Bordeaux Drive, Sunnyvale
RSVP: by June 12, on EventBrite site cnsv-marketing-clist-egrid.eventbrite.com; limited to 24
Web: cnsv-marketing-clist-egrid.eventbrite.com

This workshop is presented by **Carl Angotti**, a member of IEEE and CNSV. Carl is a successful consultant with over 25 years of consulting experience. He and other engineering consultants have used Craig's List to successfully market their services for several years and Carl has agreed to share his secrets.

One of your most important activities needed to increase business is to market your services. And it's become clear to the successful consultant members in IEEE-Consultants Network of Silicon Valley (CNSV) that marketing on Craig's List should be near the top of any successful consultant's ToDo list. So here is your chance to get even more successful than you already are.

This class is for consultants with a minimum of 1 year of experience who want to reach more potential customers.

Join Carl for a morning of "hands-on" training in Craig's List marketing for consultants. Carl will lead you step-by-step through the process of setting up a "consulting resume presence" on Craig's List.

Bring your laptop (with wireless capability). You will tap into the Cogswell WiFi and build your marketing presence in real time and by 12:30PM you will walk out with a marketing page on Craig's List that interested potential customers can use to find you and your services.

This is a big step in building or expanding your consulting business.

Notes:

- This workshop registration ends at midnight on June 12, 2009. Sorry, no walk-ins.
- Expect to receive an email with a brief homework assignment. This will give you a jump-start on understanding the process.
- This workshop is limited to 24 people so Carl can give as much one-on-one attention as is necessary for each person to complete their Craig's List marketing presence before the end of the class.
- Arrive a little before 8:30M and register, enjoy complimentary coffee and bagels, and be prepared to advance your business!
- Lunch will not be provided and the workshop will end promptly at 12:30PM.

This seminar is part of a series organized by CNSV to help its members advance their skills during these difficult times.

This event is being co-sponsored by the Santa Clara Valley Section of IEEE and the IEEE-Consultants Network of Silicon Valley (IEEE-CNSV).

Refund policy: You may request a refund up to 3 days before the event.

SCV Circuits and Systems

MONDAY June 15, 2009

Renewable Energy

Speaker: Dr. William Kao, University of California, Clean Technology Institute
Time: Networking/Pizza at 6:30 PM, Presentation at 7:00 PM
Cost: $2 donation for food
Place: Cadence Design Systems, Building 5, 655 Seely Avenue, San Jose
RSVP: not required
Web: ewh.ieee.org/r6/scv/cas

Dr. William Kao has been working in the Semiconductor and Electronic Design Automation industries for 30 years. He has a BSEE, MSEE and PhD from the University of Illinois Urbana-Champaign. He was an Adjunct Professor at UCLA Electrical Engineering Department where he taught courses in computer aided circuit design. Dr. Kao held engineering and management positions at Texas Instruments, Xerox Corporation (11 years), Cadence Design Systems (17 years), Arcadia Design and Magma Design Automation. From 1989-2000 Dr. Kao was Group Director of R&D at Cadence Analog, Mixed Signal and Custom IC group. He was VP of Engineering at Arcadia Design, and VP of Design Services and Operations at Magma Design Automation in 2000. From 2001 till February of 2008, he was Group Director of R&D at Cadence IC Digital Group responsible for the Silicon Encounter and Silicon Ensemble product lines. Dr. Kao has authored more than 40 technical papers at major conferences in the areas of circuit simulation, place and route, mixed signal test, design methodologies, and mixed signal design. Dr. Kao is a Senior member of IEEE. He was also Associate Editor of IEEE Transactions on Circuits and Systems, a member of CAS Technical Committee on Analog Signal Processing. In 2006 he was Chair of the Circuits and Systems Chapter in Silicon Valley. Dr. Kao currently teaches Renewable Energy and Business Sustainability at the Clean Technology Institute and University of California Silicon Valley extension. He is also on the Technical Advisory Board for Sigma Quest on the topics of Energy and Environment, and Quality Control and is an Energy Consultant for various companies and investment firms.

In his inaugural address on January 20 this year, President Barack Obama re-affirmed his new Administration's commitment to address climate change through additional development of renewable energy. A key passage of the speech reads: 'We will harness the sun and the winds and the soil to fuel our cars and run our factories.'

The plan is to invest in alternative and renewable energy, reduce demand for foreign oil, address climate change and create millions of new jobs. The Obama 'New Energy for America plan' aims to help create five million new jobs by strategically investing US $150 billion over the next decade, ensure 10% of US electricity comes from renewable sources by 2012, and 25% by 2025 and implement an economy-wide cap-and-trade scheme to reduce greenhouse gas emissions 80% by 2050.

This talk will cover the fundamentals, individual opportunities, challenges and limitations of each of the seven major clean, renewable energies: solar, wind, hydro, biomass, ocean (tidal, and wave), and geothermal.

Some topics covered will be concentrating solar power systems, thin film solar PV cells, biomass and biofuels, wind turbines, hydroelectric power, ocean thermal energy and ocean mechanical energy from tides and waves, and geothermal heat and electricity.

The talk will also cover briefly the global emission's Kyoto Protocol, and the California Solar Initiative.

SCV Nanotechnology

TUESDAY June 16, 2009

Nano-Solar Cells: Solar Cells of the Future with Nanotechnology

Speaker: Dr. Jeongwon Park, Applied Materials
Time: Registration and light lunch at 11:30 AM; Presentation at 12:00 Noon
Cost: $5 for IEEE members/students, $10 for non-members
Place: National Semiconductor, Bldg E-1 CMA Room, 2900 Semiconductor Drive, Santa Clara
RSVP: from the website
Web: www.ieee.org/nano

This seminar will introduce you to current solar cell technologies that are based on nanotechnology. In particular, traditional silicon-based solar cells are described and compared with more current nanocrystalline solar cells. Four types of nanotechnology based solar cells will be discussed. These include: Nano-crystalline TiO2 Dye-Sensitized Solar-Cells, Quantum dot solar cells, Nanowire solar cells, and Hybrid cells. Who may commercialize these, by when, and what major problems stand in the way will also be discussed.

Jeongwon Park received his B.E. degree in Metallurgical Engineering from Dong-A University in 1997, M.S. degree in Metallurgical Engineering from Hanyang University, South Korea in 1999 and Ph.D. from University of California, San Diego in the Materials Science and Engineering Program in 2008. Since 2008, he has been with Applied Materials where he currently is doing research on epitaxial growth in the Front End Product Group. He has been a guest researcher at Lawrence Berkeley National Labs (LBNL), and Sun Microsystems, in addition to his work at UCSD, Hanyang University, Institute for Advanced Engineering, and Seoul National University in Korea. He taught a Graduate Engineering Seminar Series at the Santa Clara University. He has published more than twenty papers.

SCV Solid State Circuits

THURSDAY June 18, 2009

A Low-Power 60GHz Transceiver with Integrated Baseband Circuitry

Speaker: Cristian Marcu, Berkeley Wireless Research Center
Time: Presentation at 6:00 PM
Cost: none
Place: National Semiconductor Building E Auditorium 2900 Semiconductor Dr., Santa Clara
RSVP: not required
Web: ewh.ieee.org/r6/scv/ssc

With mobile devices becoming more powerful and including more storage than ever before, new applications are emerging that require fast wireless data transfers while consuming very low power. This talk will present the key design techniques and challenges in implementing a low power 90nm CMOS 60GHz transceiver that includes RF, LO, PLL and BB integrated into a single chip. With a 1.2V supply the chip consumes 170mW while transmitting 10dBm and 138mW while receiving. Data transmission up to 5Gbps on each of I and Q channels has been measured, as has data reception over a 1m wireless link at 4Gbps QPSK with less than 10^{-11} BER.

Cristian Marcu (S'01) received the B.S.E.E. degree from the University of California, Irvine, in 2005 and the Masters degree in electrical engineering from the University of California, Berkeley, in 2008. He is currently pursuing the Ph.D. degree in electrical engineering at the University of California, Berkeley. In 2007, he was with Qualcomm Inc. in Campbell, working on cellular receivers. His research interests include CMOS mm-wave circuit design, and low power frequency synthesis for mm-wave applications.

SCV Signal Processing

MONDAY June 22, 2009

Adaptive Learning in a World of Projections

Speaker: Prof. Sergios Theodoridis, Technical University of Athens, Greece
Time: Fast Food & drinks at 6:30 PM; Presentation at 7:00 PM
Cost: $2 donation for food
Place: National Semiconductor, Building E Conference Center, 2900 Semiconductor Dr., Santa Clara
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/sps

Sergios Theodoridis is currently Professor of Signal Processing and Communications in the Department of Informatics and Telecommunications of the University of Athens. His research interests lie in the areas of Adaptive Algorithms and Communications, Machine Learning and Pattern Recognition, Signal Processing for Audio Processing and Retrieval. He is the co-editor of the book "**Efficient Algorithms for Signal Processing and System Identification**", Prentice Hall 1993, the co-author of the book "**Pattern Recognition**", Academic Press, 4th Ed. 2008, and the co-author of three books in Greek, two of them for the Greek Open University.

He is the co-author of four papers that have received best paper awards, including the IEEE Computational Intelligence Society Transactions on Neural Networks Outstanding Paper Award. He currently serves as Distinguished Lecturer of the IEEE Signal Processing Society. He has served as President of EURASIP and he is currently a member of the Board of Governors for the IEEE CAS Society.

He is a member of the Greek National Council for Research and Technology and Chairman of the SP advisory committee for the Edinburgh Research Partnership (ERP). He has served as vice chairman of the Greek Pedagogical Institute and he was for four years member of the Board of Directors of COSMOTE (the Greek mobile phone operating company). He is Fellow of IET, a Fellow of RSE and Fellow of IEEE.

The task of parameter/function estimation has been at the center of scientific attention for a long time and it comes under different names such as filtering, prediction, beamforming, curve fitting, classification, regression. In this talk, the estimation task is treated in the context of set theoretic estimation arguments. Instead of a single optimal point we are searching for a set of solutions that are in agreement with the available information, which is provided to us in the form of a set of training points and a set of constraints.

The goal of this talk is to present a general tool for parameter/function estimation, under a set of convex constraints, both for classification as well as regression tasks, in a time adaptive setting in (infinite dimensional) Reproducing Kernel Hilbert spaces (RKHS). Each algorithm consists of a sequence of projections, of linear complexity with respect to the number of unknown parameters. Our theory proves that the algorithm converges to the intersection of all (with a possible exception of a finite number of) the convex sets, where the required solution lies.

The work has been carried out in cooperation with Kostas Slavakis and Isao Yamada.

SF Power & Energy

WEDNESDAY June 24, 2009

Subject: Increasing Renewable Generation in California – A Key to Meeting California and US Carbon Reduction Targets

Speaker: Barney Speckman, Vice President of Energy and Power Systems, Nexant
Time: 12:00 Noon
Cost: one
Place: Pacific Gas & Electric Office, Room 305, 77 Beale St., San Francisco
RSVP: by June 22 by email to John Joven, JRJJ@PGE.COM, 415-973-4873
Web: www.e-grid.net/docs/0906-sf-pes.pdf

Barney Speckman has over 38 years of engineering, operation and contracts experience with transmission and systems control, electric production and optimization. Mr. Speckman is currently the Vice President of Nexant's Energy and Power Systems where he has been recently involved in studies related to studying the impact of higher levels of renewable generation in California including the ongoing analysis of integration requirements of 33% renewable generation that is being conducted by CAISO.

Prior to joining Nexant, Mr. Speckman worked for PG&E where he led major initiatives in generation, transmission, control, automation, power contract restructuring and industry restructuring.

The California Public Utilities Commission and the California Energy Commission unanimously agree with California Air Resources Board's recommendation to adopt requirements that by 2020 at least 33% of California's electricity needs be met by renewable resources. With Governor Schwarzenegger's executive order directing all state agencies to work toward a 33% Renewable Portfolio Standard by 2020, it is now clear that 33% renewable energy is likely to become an important part of California's clean energy future.

The implementation of a higher amount of renewable generation offers many opportunities to the industry and fosters innovation in the areas of renewable technologies, storage technologies, and smart grid technologies. However, there are significant barriers that must be overcome before the power system can be operated in a reliable and economic manner.

Barney Speckman will provide an insight into the present and future of renewable generation in California and discuss the challenges of achieving the 33% RPS target by 2020. Mr. Speckman will also discuss the results of recent studies of the impact of high levels of renewable generation, and summarize some of the ongoing analysis work looking at the reliable and economic integration of renewable generation.

THURSDAY June 25, 2009

License to Speed: Extreme-Bandwidth Packaging (plus tour)

Speaker: Sean Cahill, VP-Technology, BridgeWave Communications
Time: Pizza/drinks at 11:30 AM; Presentation at 12:00 noon; tours from 12:45 - 1:15 PM
Cost: none (includes pizza/drinks and tour)
Place: Bridgewave, 3350 Thomas Road (about two blocks from the Biltmore Hotel), Santa Clara
RSVP: via the DoubleKnot registration page, from website**; limited to first 50**
Web: www.cpmt.org/scv

Sean Cahill is VP, Technology at BridgeWave Communications where he is working on next generation millimeter-wave systems. Sean earned his MSEE/Solid State Physics from UC Santa Barbara where he fabricated some of the first surface micromachined MOEMS (Micro-opto-electro-mechanical systems). His undergraduate work entailed dual BS degrees in ECE/Signals and Systems and Biochemistry/Biophysics from UC Davis. Over his more than 20 years in industry, Sean has applied his multi-disciplinary expertise at numerous research and product development companies focused on microfabrication technologies.

Sean began his career at Exxon Research working on flat panel displays based on electrophoresis. At NovaSensor he was primarily responsible for novel devices such as microrelays, force rebalanced accelerometers, vibrating beam pressure sensors, and ion/electron beam lithography mask membranes. At Teknekron Sensor Development Sean managed the Micromachining group, pioneering chemical and biosensor platforms while developing novel mechanical sensors and microstructures. Examples of such devices include a microheater used for catalytic gas sensing, NDIR gas sensors, high dynamic range capacitive pressure sensors, SFM (scanning force microscope) probe tips which were the sharpest available, and frequency selective earthquake detectors.

After co-founding two product-based MEMS startups, Sean was recruited by Maxim Integrated Products to establish their MEMS fabrication facility and to create their patented media-compatible pressure sensor technology. Sean has served in consulting, advisory, and board member capacities at several Silicon Valley MEMS companies. He holds 23 US Patents for micromachined devices addressing many industries including automotive, process control, semiconductor, medical, and communications fields.

As device operating frequencies increase, packaging engineers look to interconnection methods that provide better signal transmission properties for high-volume applications. Next-generation interconnect approaches such as wireless and optical are areas garnering increasing research dollars, but are in practicality many years away. Flip-chip is limited as an approach because it does not address cross-talk issues without numerous extra bumps dedicated to shielding. These approaches are considerably more expensive and less flexible than wire bonding, the dominant player, either because of tooling costs or added labor-intensive steps.

This talk will describe a new interconnect approach, MicroCoax, with the capability to create high-bandwidth interconnects for increasingly higher frequency digital and analog electronics systems. Prototype devices show excellent performance over DC-100+ GHz frequency range. Transmission line losses less than 0.5 dB, 160 µm pitch, and cross-talk isolation of approximately 40-50 dB from DC-50 GHz are demonstrated. The technology has implications for improved package design, and these design implications will be discussed. In particular, low-cost QFN packages capable of operating to 80 GHz and beyond will be shown. Such a package could propagate 150 Gbps data-rate signals on a single channel.

Since the package structure is broadband, it allows for a variety of chipsets to be assembled using the same process sequence and I/O configuration, thereby eliminating costly overhead. With less than 0.5dB insertion-loss and >15dB return-loss per interconnect at 50GHz, a 5x5mm microCoax QFN package allows existing bare-die only applications to enter the world of high-speed PCB assembly, significantly driving down the cost of high-frequency systems. Process technology, I/O performance, active device performance, PCB board material selection and test protocol will all be discussed.

WEDNESDAY September 9, 2009

Molecular Modification of PCB Substrates for Fine Line Patterning

Speaker: Werner Kuhr, Ph.D., VP-Research, ZettaCore, Inc., Englewood, CO
Time: Optional dinner at 6:30 PM; Presentation at 7:30 PM
Cost: $25 if reserved by Sept 7; $30 at door (no cost for presentation)
Place: Biltmore Hotel, 2151 Laurelwood Rd (Fwy 101 at Montague Expressway), Santa Clara
RSVP: via the DoubleKnot registration page, from website
Web: www.cpmt.org/scv

Werner G. Kuhr is currently Founder and Vice President of Research, ZettaCore, Inc. which supplies molecular electronic solutions to the semiconductor and microelectronics market. Previously, he was a professor of chemistry at the University of California, Riverside, where his research was focused on the development of nano-scale techniques for the design and characterization of electrochemical devices. Professor Kuhr has published over 100 scientific papers, delivered over 100 invited lectures at conferences and universities across the world, and been issued twenty-eight U.S. and international patents. He earned B.S. and M.S. degrees in Chemistry from Stevens Institute of Technology (1980-82) and earned his Ph.D. in Chemistry from Indiana University (1986). He is currently serving on the board of advisors of the College of Natural and Agricultural Sciences, University of California, Riverside. He has been the recipient of a number of awards including a Presidential Young Investigator Award from the National Science Foundation (1989); a Young Investigator Award from the Society of Electroanalytical Chemistry (1993) and the Jubilee Silver Medal from the Chromatographic Society, England (1994).

ZettaCore® has developed a new Molecular Interface™ technology, where a molecular adhesion layer is created for smooth epoxy substrates to allow the electroless deposition and electroplating of copper onto unroughened epoxy surfaces. Molecules are attached to smooth PCB substrates via a thermally-induced reaction of the molecular species with the substrate surface, after which the high affinity of the molecule-modified surface for metal ions facilitates electroless plating of the copper, which is then used as a seed layer to electroplate larger quantities of copper utilizing conventional processes. This process allowed the fabrication of PCB substrates with fine line patterning of the metal layers (e.g., 20/20, 18/18, 14/14, 12/12 microns and 8/8 microns) using only a slight modification of standard lithographic processes using the semi-additive patterning process. Good stability to HAST and other accelerated stress tests were obtained on all of these structures, indicating that treatment with the molecular adhesion process significantly improved the ability to pattern copper lines at fine line spacing. Similar results were obtained using an analogous process for the lamination of epoxy prepreg onto smooth copper surfaces.